## CLAIMS

1. A method of testing a circuit module embedded in an integrated circuit, at least some of the pins of the circuit module not being directly connected to a pin of the larger design, the method comprising:

communicating test commands and data using a board-level test protocol through a test interface by;

scanning test vector data into a scan chain associated with the inputs of the circuit module;

applying the test vector data in the scan chain as input to the circuit module; and

retrieving the output of the circuit module through the scan chain to the test interface.

2. The method of claim 1 in which communicating test commands and data includes communicating test commands and data from off the integrated circuit using five conductors including a clock conductor, a test mode conductor, a reset conductor, a data in conductor and a data out conductor.

3. The method of claim 1 further comprising converting a test vector into a series of JTAG protocol test commands and data, the JTAG command including a user defined command for defining an address for a circuit module.

4. The method of claim 3 in which converting a test vector includes maintaining timing relationships actions initiated by the test commands.

5. The method of claim 1 in which scanning test vector data into a scan chain includes scanning the test vector data to a single boundary scan register, the single boundary scan register being associated with the circuit module under test.

6. The method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary scan register to the test interface without scanning the output through a second boundary scan ring.

7. The method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary scan register through at least one dedicated output conductor.

8. A system for testing one or more of multiple circuit modules embedded in an integrated circuit, comprising:

a test controller for accepting serial data and control signals from outside the integrated circuit in accordance with a test protocol that corresponds to a board level test protocol , the controller including;

a first selector for selecting one of the multiple circuit modules for testing, control signals being transmitted to only the selected one of the test modules; and

a second selector for selecting output from the selected one of the circuit modules;

and

a boundary scan register corresponding to each of the one or more circuit modules, the boundary scan register providing input to circuit modules from the controller in a test mode and from an operating input when in operating mode.

9. The system of claim 8 in which the test controller includes logic for using serial data and control signals in accordance with a JTAG protocol.

10. The system of claim 8 further comprising multiple sets of four conductors, one set connecting the selector to each of the boundary scan registers.

11. The system of claim 10 in which the four conductors include a clock line, an update line, a mode line, and a data capture line.

12. The system of claim 10 further comprising a data input line that connects from the test controller to every boundary scan register.

13. The system of claim 10 further comprising multiple data output lines, each connecting from a different boundary scan register to the second selector.

14. The system of claim 8 in which each boundary scan register includes test logic for each input pin, output pin, and bi-directional pin of the corresponding circuit module, the test logic for each input pin including a latch for scanning in data, a latch for applying data, and a data selector for selectively conveying data from the latch to the input pin.

15. The system of claim 8 in which each boundary scan register includes test logic for each input pin, output pin, and bi-directional pin of the corresponding circuit module, the test logic for each output pin including a latch for scanning data and a selector for selectively storing in the latch output from the output pin or data from the scan chain.

16. The system of claim 8 in which each boundary scan register includes test logic for each input pin, output pin, and bi-directional pin of the corresponding circuit module, the test logic for each bi-directional pin including tri-state buffer.

17. The system of claim 8 further comprising five conductors for conveying data and control signals from the test controller to the test interface.

18. The system of claim 17 in which the five conductors include a data in line, a data out line, a clock line, a test mode set line, and a reset line.

19. A system for testing one or more of multiple circuit modules embedded in an integrated circuit, comprising:

a test controller for accepting serial data and control signals from a test interface in accordance with a test protocol that corresponds to a board level test protocol; and

a boundary scan register corresponding to each of the one or more circuit modules, the boundary scan ring providing input to circuit modules from the controller in a test mode and from an operating input when in operating mode.

20. The system of claim 19 in which the test controller includes logic for accepting serial data and control signals in accordance with a test protocol that corresponds to a JTAG protocol.

21. The system of claim 19 in which the test controller includes a selector for selecting one of the multiple circuit modules for testing, control signals being transmitted to only the selected one of the test modules.

22. The system of claim 19 in which a test controller for accepting serial data and control signals from a test interface in accordance with a test protocol that corresponds to a board level test protocol includes a selector for selecting output from the selected one of the circuit modules.

23. A system for testing one or more of multiple circuit modules embedded in an integrated circuit, comprising:

a test controller for accepting serial data and control signals from outside the integrated circuit, the test controller including logic for communicating with outside the integrated circuit using a clock line, a reset line, a test mode line, a data-in line, and a data-out line;

one or more multiple boundary scan register, each boundary scan register corresponding to one of the circuit modules, each boundary scan register providing input to the corresponding circuit module from the test controller when the integrated circuit is in a test mode and from an operating input when in the integrates circuit is in an operating mode; and

conductors for the test controller to communicate with the boundary scan registers, the conductors including a data-in line, a data-out line, a clock line, a mode line to indicate whether the integrated circuit module is in test mode or operating mode, an output data capture line indicating that output from the circuit module is to be captured, an input application line to indicate that input data in the boundary scan register is to be applied to the inputs of the circuit module.

24. The method of claim 23 in which the test controller includes logic for accepting commands and data formatted in a JTAG protocol.

25. A method of testing a circuit module embedded in an integrated circuit design, at least some of the pins of the circuit module not being directly connected to a pin of the larger design, test commands and data being communicated to the circuit module using five conductors including a clock conductor, a test mode conductor, a reset conductor, a data in conductor, and a data out conductor, the method comprising;

scanning through the data in conductor commands and data into a scan chain associated with the inputs of the circuit module;

applying the data in the scan chain as input to the circuit module; and

retrieving through the data out conductor output of the circuit module through the scan chain to the test interface.